TOSHIBA Multi-Chip Transistor
Silicon NPN Epitaxial Type, Field Effect Transistor Silicon N Channel MOS Type

TPCP8H01

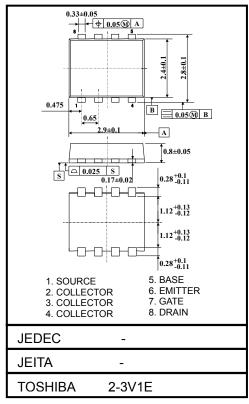
HIGH-SPEED SWITCHING APPLICATIONS LORD SWITCHING APPLICATIONS STROBE FLASH APPLICATIONS

- Multi-chip discrete device; built-in NPN transistor for main switch and N-ch MOS FET for drive
- High DC current gain: $h_{FE} = 250 \text{ to } 400 \text{ (IC} = 0.5 \text{ A)}$ (NPN transistor)
- Low collector-emitter saturation voltage: VCE (sat) = 0.13 V (max)(NPN transistor)
- High-speed switching: $t_f = 25 \text{ ns (typ.)}$ (NPN transistor)

Absolute Maximum Ratings (Ta = 25°C)

Transistor

Characteristics		Symbol	Rating	Unit	
Collector-base voltage		V _{CBO}	100	V	
Collector-emitter voltage		V _{CEX}	80	V	
		V _{CEO}	50		
Emitter-base voltage		V _{EBO}	6	V	
Collector current	DC (Note 1)	Ic	5.0	Α	
	Pulse (Note 1)	I _{CP}	7.0		
Base current		Ι _Β	0.5	Α	
Collector power dissipation (NPN)		P _C (Note 2)	1.0	W	
Junction temperature		Tj	150	°C	

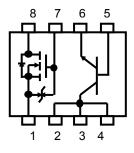


Weight: 0.017g (Typ.)

MOS FET

Characteristics		Symbol	Rating	Unit	
Drain-Source Voltage		V_{DSS}	20	V	
Gate-Source Voltage		V_{GSS}	±10	V	
Drain Current	DC	ΙD	100	mA	
	Pulse	I _{DP}	200	IIIA	
Channel Temperature		T _{ch}	150	°C	

Circuit Configuration



- Note 1: Ensure that the junction (channel) temperature does not exceed 150°C.
- Note 2: Device mounted on a glass-epoxy board (FR-4, 25.4 × 25.4 × 1.6 mm, Cu area: 645 mm²)
- Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

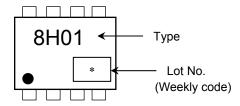
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Please handle with caution.

Common Absolute Maximum Rating (Ta = 25°C)

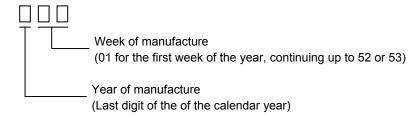
Characteristics	Symbol	Rating	Unit
Storage temperature range	T _{stg}	-55 to 150	°C

Marking (Note 4)



Note 4: The mark "●" on the lower left of the marking indicates Pin 1.

* Weekly code (three digits)



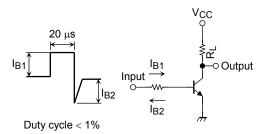
Electrical Characteristics (Ta = 25°C)

Transistor

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Collector cut-off current		I _{CBO}	V _{CB} = 100 V, I _E = 0	_	_	100	nA
Emitter cut-off current		I _{EBO}	$V_{EB} = 6 \text{ V}, I_{C} = 0$	_	_	100	nA
Collector-emitter breakdown voltage		V (BR) CEO	I _C = 10 mA, I _B = 0	50	_	_	V
DC current gain		h _{FE} (1)	$V_{CE} = 2 \text{ V}, I_{C} = 0.5 \text{ A}$	250	_	400	
		h _{FE} (2)	V _{CE} = 2 V, I _C = 1.6 A	100	_	_	
Collector-emitter saturation voltage		V _{CE} (sat)	$I_C = 1.6 \text{ A}, I_B = 53 \text{ mA}$	_	80	130	mV
Base-emitter saturation voltage		V _{BE} (sat)	I _C = 1.6 A, I _B = 53 mA	_	0.8	1.1	V
Collector output capacitance		C _{ob}	V _{CB} = 10 V, I _E = 0, f = 1 MHz	_	22	_	pF
Switching time	Rise time	t _r	See Figure 1 circuit diagram.	_	65	_	
	Storage time	t _{stg}	$V_{CC} = 24 \text{ V}, R_L = 15 \Omega$	_	500	_	ns
	Fall time	t _f	$I_{B1} = -I_{B2} = 53 \text{ mA}$	_	25	_	

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Figure 1 Switching Time Test Circuit & Timing Chart



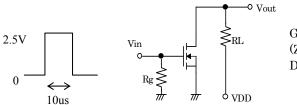
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MOS FET

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$	_	_	±1	μΑ
Drain-Source breakdown voltage		V _{(BR)DSS}	$I_D = 0.1 \text{ mA}, V_{GS} = 0$	20	_	_	V
Drain cut-off current		I _{DSS}	V _{DS} = 20 V, V _{GS} = 0	_	_	1	μΑ
Gate threshold voltage		V th	$V_{DS} = 3 \text{ V}, I_D = 0.1 \text{ mA}$	0.6	_	1.1	V
Forward transfer admittance		Yfs	$V_{DS} = 3 \text{ V}, I_D = 10 \text{ mA}$	40	_	_	mS
Drain-Source ON resistance		R _{DS(ON)}	$I_D = 10 \text{ mA}$, $V_{GS} = 4.0 \text{ V}$	_	1.5	3	Ω
			$I_D = 10 \text{ mA}$, $V_{GS} = 2.5 \text{ V}$	_	2.2	4	
			I _D = 1 mA , V _{GS} = 1.5 V	_	5.2	15	
Input capacitance		C _{iss}	V _{DS} = 3 V, V _{GS} = 0, f= 1 MHz	_	9.3	_	pF
Reverse transfer capacitance		C _{rss}		_	4.5	_	
Output capacitance		Coss		_	9.8	_	
Switching time	Turn-on time	t _{on}	See Figure 2 circuit diagram.	_	70	_	
	Turn-off time	t _{off}	$V_{DD} = 3 \text{ V}, R_L = 300 \Omega$	_	125	_	ns
			V _{GS} = 0 to 2.5 V				

Figure 2 Switching Time Test Circuit & Timing Chart



Gate Pulse Width 10 μ s, tr,tf<5ns (Zout=50 Ω), Common Source,Ta=25°C Duty Cycle<1%

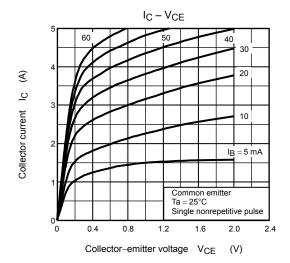
Precautions

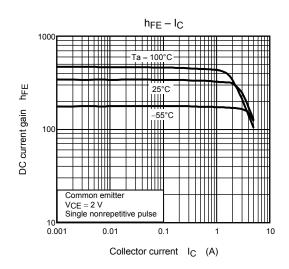
 V_{th} can be expressed as the voltage between gate and source when the low operating current value is ID=100 μA for this product. For normal switching operation, V_{GS} (on) requires a higher voltage than V_{th} and V_{GS} (off) requires a lower voltage than V_{th} .

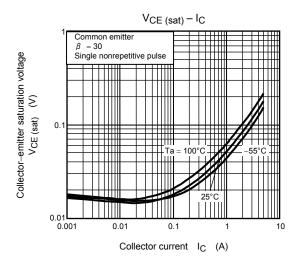
(The relationship can be established as follows: $V_{GS \text{ (off)}} < V_{th} < V_{GS \text{ (on)}}$)

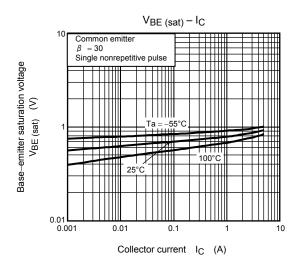
Please take this into consideration when using the device. The $V_{\rm GS}$ recommended voltage for turning on this product is $2.5~{\rm V}$ or higher.

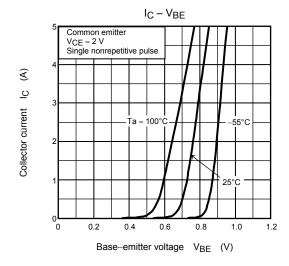
NPN

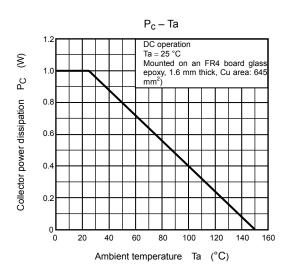


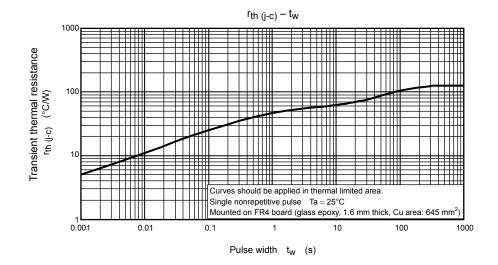


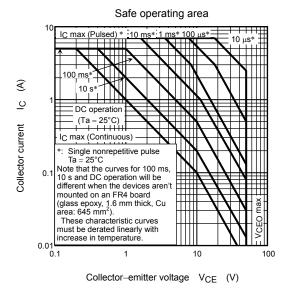




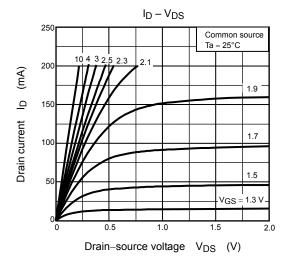


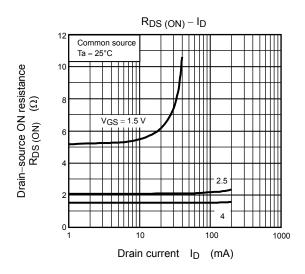


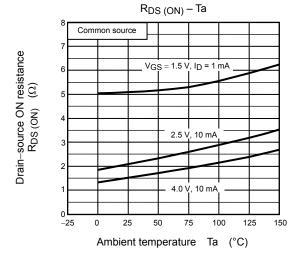


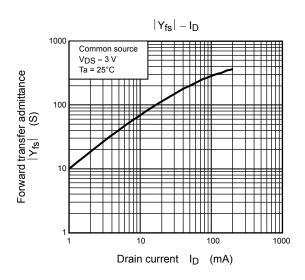


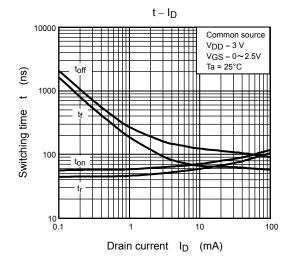
Nch-MOS

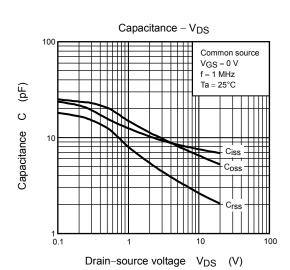




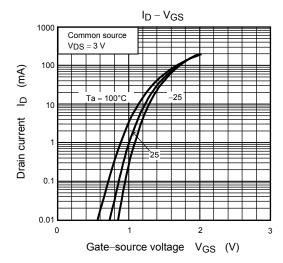


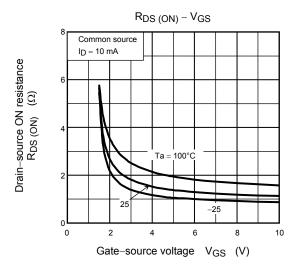


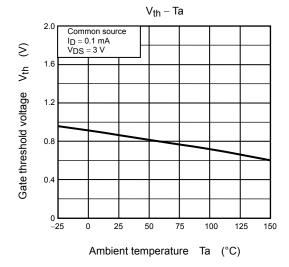


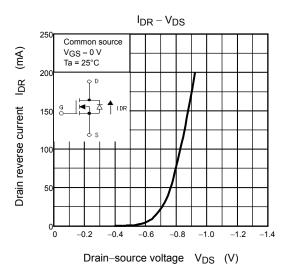


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